CLAIMS

1. A digital data processing device, comprising:

instruction logic which selects and decodes instructions for execution;

execution logic which executes instructions;

a first cache for temporarily storing data, said first cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank; and

wherein a respective bank predict value is associated with each of at least some instructions accessing said first cache, each said bank predict value predicting a bank of said first cache to be accessed by its associated instruction; and

wherein said instruction logic selects multiple instructions for concurrent execution, said instruction logic using said bank predict values of said instructions to select multiple instructions which access said first cache for concurrent execution.

2. The digital data processing device of claim 1, further comprising a second cache for temporarily storing data, wherein said second cache stores instructions executable by said execution logic and said first cache stores data other than instructions, and wherein said bank predict values are stored in said second cache.

3. The digital data processing device of claim 1, wherein each said bank of said first cache contains a plurality of read ports and at least one write port.

4. The digital data processing device of claim 1,

wherein a respective confirmation value is associated with each said instruction with which a bank predict value is associated, each confirmation value reflecting a degree of confidence in the respective bank predict value; and

wherein said instruction logic uses both said bank predict values and said confirmation values of said instructions to select multiple instructions which access said first cache for concurrent execution.

5. The digital data processing device of claim 4,

wherein said digital data processing device dynamically maintains said confirmation values.

6. The digital data processing device of claim 5,

wherein each said confirmation value is a counter which is incremented for each correct bank prediction and decremented for each incorrect bank prediction.

7. The digital data processing device of claim 1, further comprising:

feedback logic which maintains bank prediction history data in a form accessible to a programmer, said bank prediction history data recording the performance of bank predictions by said bank predict values during execution of a computer program.

8. The digital data processing device of claim 1,

wherein said instruction logic concurrently selects and decodes instructions for execution from a plurality of threads.

9. The digital data processing device of claim 1,

wherein said digital data processing device is implemented in a single semiconductor chip.

10. A computer system, comprising:

a memory;

at least one processor, said processor communicating with said memory over at least one communications path, said processor including instruction logic for selecting and decoding instructions for execution, and execution logic for executing instructions

a first cache coupled to said processor and temporarily storing data from said memory, said first cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank; and

wherein a respective bank predict value is associated with each of at least some instructions accessing said first cache, each said bank predict value predicting a bank of said first cache to be accessed by its associated instruction; and

wherein said instruction logic selects multiple instructions for concurrent execution, said instruction logic using said bank predict values of said instructions to select multiple instructions which access said first cache for concurrent execution.

11. The computer system of claim 10, further comprising a second cache for temporarily storing data, wherein said second cache stores instructions executable by said processor and said first cache stores data other than instructions, and wherein said bank predict values are stored in said second cache.

12. The computer system of claim 10, wherein each said bank of said first cache contains a plurality of read ports and at least one write port.

13. The computer system of claim 10,

wherein a respective confirmation value is associated with each said instruction with which a bank predict value is associated, each confirmation value reflecting a degree of confidence in the respective bank predict value; and

wherein said instruction logic uses both said bank predict values and said confirmation values of said instructions to select multiple instructions which access said first cache for concurrent execution.

14. The computer system of claim 13,

wherein said computer system dynamically maintains said confirmation values.

15. The computer system of claim 14,

wherein each said confirmation value is a counter which is incremented for each correct bank prediction and decremented for each incorrect bank prediction.

16. The computer system of claim 10, further comprising:

feedback logic which maintains bank prediction history data in a form accessible to a programmer, said bank prediction history data recording the performance of bank predictions by said bank predict values during execution of a computer program.

17. The computer system of claim 10,

wherein said instruction logic concurrently selects and decodes instructions for execution from a plurality of threads.

18. The computer system of claim 10,

wherein said computer system comprises a plurality of caches at different cache levels, said first cache being at a level closest said processor.

19. The computer system of claim 10,

wherein said computer system comprises a plurality of said processors, each processor being coupled to a respective first cache, and wherein said bank predict values associated with instructions are maintained in a location accessible to each of said plurality of processors.

20. A digital data processing device, comprising:

a cache for temporarily storing data, said cache comprising a plurality of banks, each bank containing at least one respective access port for accessing data in the bank;

execution logic for executing multiple instructions concurrently;

instruction logic for selecting and dispatching sets of instructions which can be concurrently executed without conflict by said processing device, wherein at least some of said instructions access said cache, said instruction logic using a respective bank predict value associated with at least some instructions accessing said cache to predict whether multiple instructions accessing said cache can be concurrently executed without conflict by said processing device.